1. (Previously Presented) A semiconductor integrated circuit, comprising:

a ROM having bit lines extending in a first direction in a first layer; and

a conductive line arranged in a second layer, located above the first layer, wherein the conductive line partially extends in a second direction, which is orthogonal to the first direction, to pass across the bit lines, and is shaped to be a step form having a part extending in the first direction.

2-3. (Cancelled)

4. (Original) A semiconductor integrated circuit, according to claim 1, wherein

the conductive line has two ends extending toward upper and lower portions of a ROM block, respectively.

5. (Original) A semiconductor integrated circuit, according to claim 1, wherein

the conductive line has two ends extending toward a right upper portion and a left lower portion of a ROM block, respectively.

6. (Original) A semiconductor integrated circuit, according to claim 1, wherein

the conductive line has two ends both extending toward the same side of a ROM block.

7. (Cancelled)

8. (Currently Amended) A smart card, comprising:

a ROM;

a CPU using a runnable program fixed at the time of the manufacture of a component in the ROM; and

a RAM, which enables the CPU to enter and use temporary data during its operation, wherein the ROM has bit lines extending in a first direction in a first layer; and a conductive line arranged in a second layer, located above the first layer, the conductive line partially extending in a second direction, which is orthogonal to the first direction, to pass across the bit lines, wherein the conductive line is shaped to be a step form having a part extending in the first direction.

9. (Cancelled)

10. (Cancelled)

11. (Original) A smart card according to claim 8, wherein the conductive line has two ends extending toward upper and lower portions of a ROM block, respectively.

12. (Currently Amended) ~~A smart card according to claim 8,~~ A smart card, comprising:

a ROM;

a CPU using a runnable program fixed at the time of the manufacture of the component in the ROM; and

a RAM enables the CPU to enter and use temporary data during its operation, wherein

the ROM has bit lines extending in a first direction in a first

layer; and a conductive line arranged in a second layer, located above the first layer, the conductive line partially extending in a second direction, which is orthogonal to the first direction, to pass across the bit lines, wherein

the conductive line has two ends extending toward a right upper portion and a left lower portion of a ROM block, respectively.

13. (Currently Amended) A smart card according to claim 12~~0~~, wherein the conductive line has two ends both extending toward the same side of a ROM block.

14. (Cancelled)

15. (Original) A method for designing a semiconductor integrated circuit according to claim 1, comprising the steps of:

providing bit lines for a ROM extending in a first direction in a first layer;

providing a conductive line arrangement in a second layer, located above the first layer, by an automatic design technique; and

rearranging the conductive line by a manual design technique so that the conductive line partially extends in a second direction, which is orthogonal to the first direction, to pass across the bit lines.

16. (Original) A method according to claim 15, wherein the conductive line is shaped to be a step form having a part extending in the first direction.

17. (Previously Presented) A method according to claim 15, wherein the conductive line is shaped so as to pass across the bit lines two or more times.

18. (Original) A method according to claim 15, wherein the conductive line has two ends extending toward upper and lower portions of a ROM block, respectively.

19. (Original) A method according to claim 15, wherein the conductive line has two ends extending toward a right upper portion and a left lower portion of a ROM block, respectively.

20. (Original) A method according to claim 15, wherein the conductive line has two ends both extending toward the same side of a ROM block.

21. (Currently Amended) ~~A semiconductor integrated circuit according to claim 21,~~ A semiconductor integrated circuit, comprising:

a ROM having bit lines extending in a first direction in a first layer; and

a conductive line arranged in a second layer, located above the first layer, wherein the conductive line partially extends in a second direction, which is orthogonal to the first direction, to pass across the bit lines, and is shaped to pass across the bit lines two or more times, wherein the conductive line has two ends extending toward a right upper portion and a left lower portion of a ROM block, respectively.

22. (Cancelled)

23. (Currently Amended) A semiconductor integrated circuit, comprising:

a ROM having bit lines extending in a first direction in a first layer; and

a conductive line arranged in a second layer, located above the first layer, wherein the conductive line partially extends in a second direction, which is orthogonal to the first direction, to pass across the bit lines, and is shaped to pass across the bit lines two or more times, and wherein the conductive line has two ends both extending toward the same side of a ROM block.